Low power 1 bit-cmos Full adder based on Reduction of parasitic capacitance through Layout optimization

Dayadi.Lakshmaiah[1] Dr.M.V.Subramanyam [2] Dr.K.Satya Prasad[3]

[1]Ph.D Research scholar ECE Department, JNTU, Kakinada, Asso.pro ,NIET ,HYD India. laxmanrecw@gmail.com

[2]Principal and Professor of ECE Department, Santhi Ram Engineering College, Nandyala, India. mvsraj@yahoo.com

[3]Professor of ECE Department and Rector, JNTU Kakinada, Kakinada, India. prasad_kodati@yahoo.co.in

***Abstract**:-*

The Aim of this paper is to calculate the MOSFET parasitic capacitances, and then based on the results obtained we can further see the impact of MOSFET physical parameters on these parasitic capacitances. These capacitances have a direct impact in the speed of operation of MOSFET circuits. Therefore, in order to increase the speed of operation, it is necessary that the parasitic capacitances are reduced to a minimum possible level that the technological process allows. We have analyzed the different types of capacitance effect as a function of the MOSFET dimensions. 0perating an Integrated circuit at the prescribed Reduction of parasitic capacitance through Layout optimization is preferable for reliable circuit operation. In this work we proposed to design 1 –bit full adder by "Reduction of parasitic capacitance through Layout optimization" we measured pars tic capacitance, power consumption, leakage current, layout area, Delay ,etc parameters. The results are compared with the previous work and shown that Power is saved 63%, 55% of leakage current , 72% of total capacitance at input A, 63% of total capacitance at input B, 74% of total capacitance at input C, 86% of total capacitance at sum, , 86%of total capacitance at carry, 88% of gate capacitance,77% of diffusion capacitance ,86% of metal capacitance and 100% of crosstalk capacitance and 99% of delay and 71% of Area. We have performed simulations using 90 Nanometer (nm) Micro wind 3 CMOS layout CAD Tool for design.

Key words: layout optimization, total capacitance, diffusion capacitance, gate capacitance, metal capacitance, crosstalk capacitance, leakage current (Ion+Ioff), Area,Delay

1. Introduction:-

Power dissipation has become a prime constraint in high performance applications, especially in portable and battery operated ASIC systems so it is necessary to reduce power consumption. Power consumption is proportional to square of supply voltage [1] cmos circuits the cost of lower supply voltage is lower performance. Scaling the threshold voltage can limit this performance loss to some extent but results in increased leakages [2] The advantage of GDI technique two-transistor implementation of complex logic functions and in-cell swing restoration under certain operating conditions, are unique within existing low-power design techniques.[3] Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground) [4], this device is turned off in the sleep mode to cut-off the leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance [5], [6], [7], [8]. With the scaling of transistor dimensions extrinsic, or lay- out dependent, parasitic capacitance contributions, such as poly-to-contact coupling, as well as corner capacitance, become more and more important with respect to intrinsic contributions [10]. Accumulated systematic numerical data that clarify the dependence of the capacitance on gate length L_G, gate electrode thickness t_p, and gate oxide thickness t_{ox}[11].

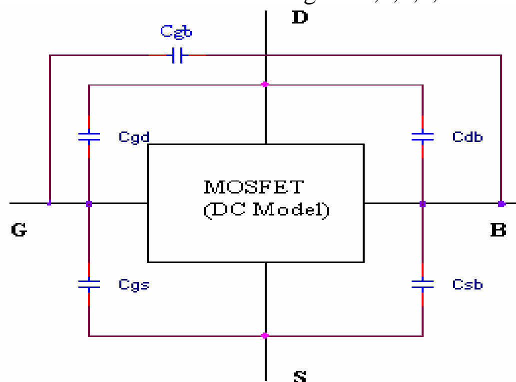
2. Proposed work:-

2.1. Parasitic capacitance:-

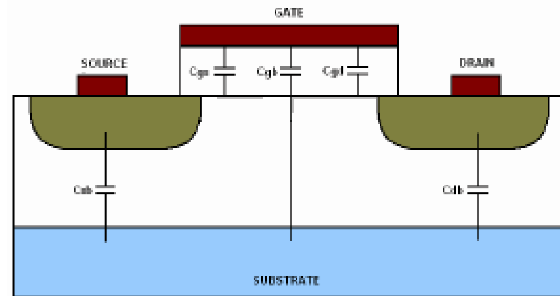
Any two conductors separated by insulator have capacitance; gate to channel capacitor is very important Logic-cell delay results from transistor resistance, transistor (intrinsic) parasitic capacitance, and load (extrinsic) capacitance. When one logic cell drives another, the parasitic input capacitance of the driven cell becomes the load capacitance of the driving cell and this will determine the delay of the driving cell. An unwanted coupling from a neighboring signal wire to a N/W node introduces an interference that is generally called cross talk. Cross talk making wire delay more, more unpredictable.

In electrical circuits, parasitic capacitance, stray capacitance or, when relevant, self-capacitance (of an inductor), is an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other. All actual circuit elements such as inductors, diodes, and transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. In addition, there is always non-zero capacitance between any two conductors; this can be significant at higher frequencies with closely spaced conductors, such as wires or printed circuit board traces.

Based on physical structure of MOSFET, its parasitic capacitances can be classified into two major groups:– the gate capacitive effect (indicated by C_{ox}) and– junction capacitances *drain-body* and *source-body*.These two capacitive effects can be modeled by including capacitances in the MOSFET model between its four terminals, G, D, S, and B as shown in Fig.2. There will be five capacitances: C_{gs}, C_{gd}, C_{gb}, C_{sb} and C_{db} where the subscripts indicate the terminals shown in below figures1,2,3,4,5.



Figure(1)



Fig(2)

- Three main forms:
  - Gate capacitance (gate of transistor)
  - Diffusion capacitance (drain regions)
  - Routing capacitance (metal, etc.)

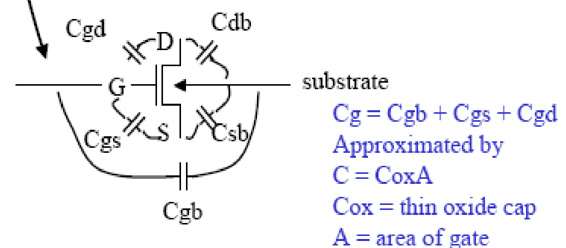
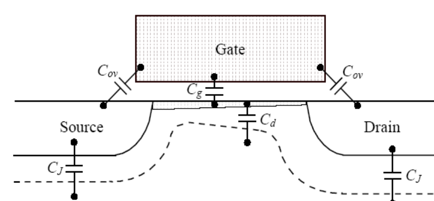
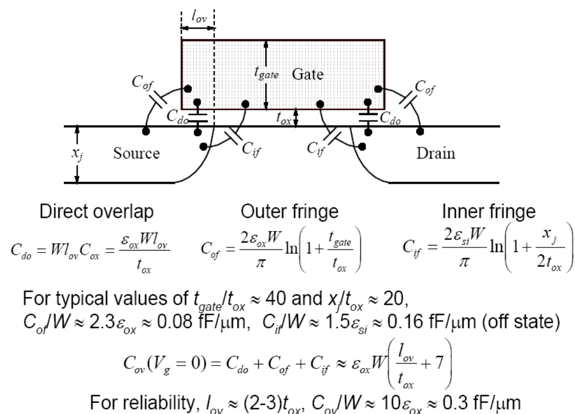


Figure (3)



- Intrinsic capacitance: $C_g = WLC_{ox}$ $\quad C_g = \frac{2}{3}WLC_{ox}$
- Parasitic capacitances:
  - Depletion capacitance $C_d = \varepsilon_s WL / W_{dm}$
  - Overlap capacitance
  - Junction capacitance $C_j = \varepsilon_{si} Wd / W_{dj} = Wd\sqrt{\frac{\varepsilon_{si} q N_a}{2(\psi_{bi} + V_j)}}$

Figure (4)



Figure(5)

3. Performance Analysis and Simulation Results:-

parameter	Reference paper.12	Reference paper.13	Proposed work	% saved
Power (μw)	9.417	5.4	3.5	63
Area(μm^2)	306	504	92	71
Leakage current(Ion+Ioff)A	1.65mA+40nA	1.65mA+40nA	0.64mA+22nA	55
Point A Total Capacitance(fF)	6.39	15.06	1.82	72
Metal capacitance	1.43	2.93	0.25	
Crosstalk capacitance	0.02	0.01	0.00	
Diffusion capacitance	0.09	0.07	0.04	
Gate capacitance	4.87	12.06	1.53	
Point B Total capacitance(fF)	7.79	17.94	2.89	63
Metal capacitance	2.84	5.91	1.12	
Cross talk capacitance	0.08	0.04	0.00	
Diffusion capacitance	0.24	0.20	0.08	
Gate capacitance	4.71	11.84	1.68	
Point C Total capacitance(fF)	7.50	10.07	1.99	74

Metal capacitance Cross talk capacitance Diffusion capacitance Gate capacitance	2.48 0.05 0.15 4.87	5.44 0.03 0.13 4.50	0.36 0.00 0.04 1.59	
Carry Total capacitance (fF) Metal capacitance Cross talk capacitance Diffusion capacitance Gate capacitance	2.92 2.08 0.02 0.24 0.00	5.48 5.26 0.01 0.22 0.00	0.41 0.33 0.00 0.08 0.00	86
Sum Total capacitance(fF) Metal capacitance Cross talk capacitance Diffusion capacitance Gate capacitance	2.71 2.47 0.03 0.24 0.00	4.87 4.46 0.02 0.20 0.00	0.40 0.32 0.00 0.08 0.00	86
Delay	0.47	0.66ns	0.22ns	72

f means femoto (10^{-15})

Table.1 . Comparison of results previous work and proposed work.

The results are compared with the previous work we shown that table.1 that Power is saved 63%, 55% of leakage current , 72% of total capacitance at input A, 63% of total capacitance at input B, 74% of total capacitance at input C, 86% of total capacitance at sum, , 86%of total capacitance at carry, 88% of gate capacitance,77% of diffusion capacitance ,86% of metal capacitance ,100% of crosstalk capacitance ,72% of delay, and 71% of Area .Simulation results Shown in below figures (4-12) We have performed simulations using 90 Nanometer (nm) Micro wind 3 CMOS layout CAD Tool for design.

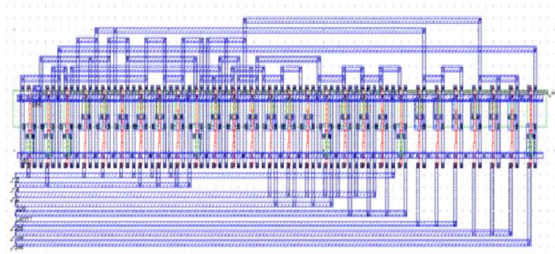


Fig (4) Reference .12 layout design

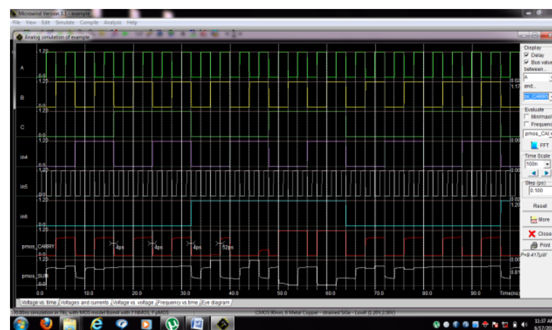


Fig (5) Reference .12 power report

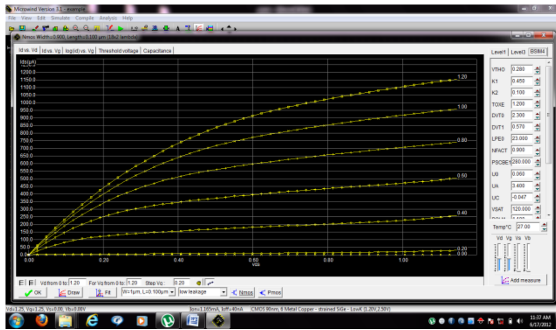


Fig (6) Reference .12 leakage current

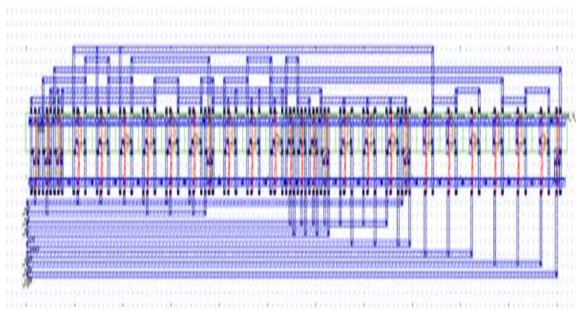


Fig (7) Reference.13 layout design

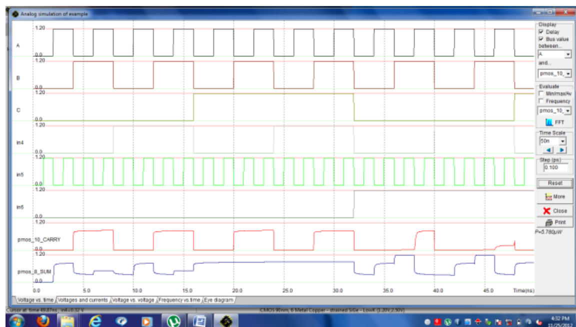


Fig (8) Reference .13 power report

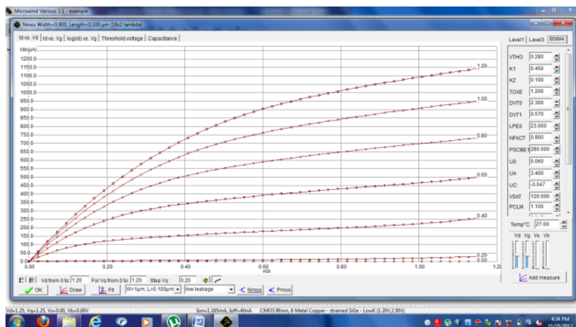


Fig (9) Reference .12 leakage current

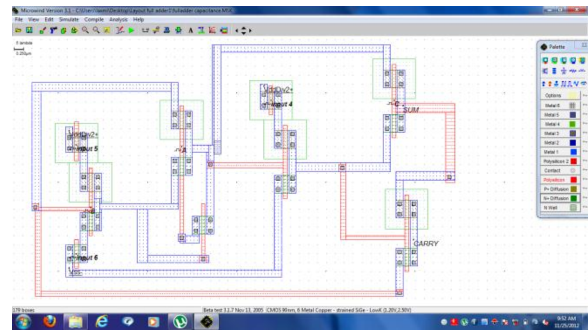


Fig (10) Proposed work Layout optimization

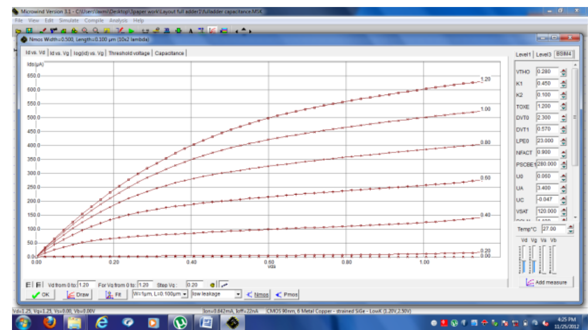


Fig (11) Proposed work leakage current

Fig (12) Proposed work power report

4. Conclusion:-

The results are compared with the previous work and we shown that Power is saved 63%, 55% of leakage

current , 72% of total capacitance at input A, 63% of total capacitance at input B, 74% of total capacitance at input C, 86% of total capacitance at sum, , 86%of total capacitance at carry, 88% of gate capacitance,77% of diffusion capacitance ,86% of metal capacitance and 100% of crosstalk capacitance , 99% of delay, and 71% of Area. We have performed simulations using 90 Nanometer (nm) Micro wind 3 CMOS layout CAD Tool for design. Further power can be saved by using high and low threshold voltage and by using various parameters through Layout optimization.

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Dayadi.Lakshmaiah is currently pursuing PhD Research scholar ECE Department, JNTUniversity, Kakinada, and *working as Asso.professor Nizam Institute of Engineering and Technology Deshmuki Hyderabad .AndraPradesh (State), India. He Received B.Tech Degree in ECE From National Institute of Technology, Warangal (RECW) and M.Tech (DSCE) Degree From JNTUA Anantapur Andhra Pradesh He has published 8 International Journals..*

Dr.M.V.Subramanyam Professor of ECE, currently working as Principal of Santhiram Engineering College Nandyal, Andhra Pradesh, India. He has 22 years of Experience in Teaching. He authored 4 text books, STLD, Computer Networks, Basic Electronics and Microprocessor& Microcontroller Interfacing and Application. He published more than 48 Technical papers in various National and International Journals and Conferences', He has an Editorial Member for the 4 International journal and 3 National Journals. "His Area of interest is Adhoc Wireless Networks, Cellular and Mobile Communications. He has Received B.Tech & M.Tech in ECE from JNTU, Hyderabad, PhD (Adhoc wireless Networks) Degree from JNTUH, Hyderabad, Andhra Pradesh, India. He has completed 5 research projects sponsored by the IE(I), India and currently one research project in hand which is funded by AICTE, New Delhi.

Dr. K. Sathaya Prasad Professor of ECE is currently working as Rector of JNTUK, Kakinada. He has more than 32 years of experience in teaching and 25 years of R & D. He is an expert in Digital Signal Processing. He has Guided to 10Ph.D's and guiding 10Ph.D scholars. He authored Electronic Devices and Circuits text book. He held different positions in his career like Head of the Department, vice principal, and principal for JNTU Engineering College (JNTUK). He published more than 60 technical papers in National and International Journals and conferences. He also received best Teacher Award from Govt of Andhra Pradesh in 2010. He is Received B.Tech Degree in ECE from JNTUA Anantapur, M.E (Communication Systems) Degree from University of Madras, and Ph.D (signal Processing) Degree from the Indian Institute of Technology Madras, India.